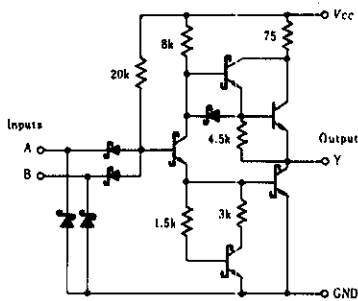


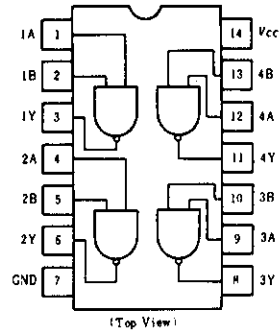
HD74LS00

● Quadruple 2-input Positive NAND Gates

■ CIRCUIT SCHEMATIC (1/4)



■ PIN ARRANGEMENT



■ ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ*	max	Unit	
Input voltage	V_{IH}		2.0	—	—	V	
	V_{IL}		—	—	0.8	V	
Output voltage	V_{OH}	$V_{CC} = 4.75\text{V}$, $V_{IL} = 0.8\text{V}$, $I_{OH} = -400\mu\text{A}$	2.7	—	—	V	
	V_{OL}	$V_{CC} = 4.75\text{V}$, $V_{IH} = 2\text{V}$	$I_{OL} = 8\text{mA}$	—	—	0.5	V
			$I_{OL} = 4\text{mA}$	—	—	0.4	
Input current	I_{IH}	$V_{CC} = 5.25\text{V}$, $V_I = 2.7\text{V}$	—	—	20	μA	
	I_{IL}	$V_{CC} = 5.25\text{V}$, $V_I = 0.4\text{V}$	—	—	-0.4	mA	
	I_I	$V_{CC} = 5.25\text{V}$, $V_I = 7\text{V}$	—	—	0.1	mA	
Short-circuit output current	I_{OS}	$V_{CC} = 5.25\text{V}$	-20	—	-100	mA	
Supply current	I_{CCH}	$V_{CC} = 5.25\text{V}$	—	0.8	1.6	mA	
	I_{CCL}	$V_{CC} = 5.25\text{V}$	—	2.4	4.4	mA	
Input clamp voltage	V_{IK}	$V_{CC} = 4.75\text{V}$, $I_{IH} = -18\text{mA}$	—	—	-1.5	V	

* $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$

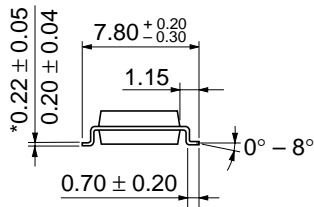
■ SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$	—	9	15	ns
	t_{PHL}		—	10	15	ns

Note) Refer to Test Circuit and Waveform of the Common Item



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g



Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

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